# Radiation-Tolerant Techniques for Digital Radio and Other Applications

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Human missions beyond low-Earth orbit will see a reduction in the ability to find usable commercial chipsets for advanced protocols. While total dose effects and latchup are reduced in deep submicron low-voltage processes, single event effects susceptibility greatly increases. The burst nature of deep space radiation from solar events produces occasional error rates that overwhelm system-level redundancy approaches.

Large-capacity reconfigurable Static Random Access Memory (SRAM)-based Field Programmable Gate Arrays (FPGA), which are sometimes used as an alternative to chipsets, are also not likely to be reliable in space. Ninety percent of such devices consist of highly susceptible configuration memory. Errors in this memory change the function of the device, calling internal redundancy schemes into question. Finding configuration memory errors by scrubbing involves considerable delay during which time the chip is emitting errors that may propagate into the system or chip state vector and become undetectable when correct operation is restored.

The work described here builds on and adds to NASA's long involvement with Radiation Hardened by Design (RHBD) techniques for Complementary Metal-Oxide Semiconductor (CMOS). The results can be applied directly to make reasonably low-cost, reliable, application-specific integrated circuits (ASICs). Our work also includes investigation of computationally efficient techniques allowing radio algorithms to be implemented in devices, whether FPGA or ASIC, with smaller gate counts and higher reliability.

## Transition and Gate/Guard Gate Based Flip-Flop Designs

Design of latch or flip-flop circuits for Single Event Upset immunity has evolved over many years. Early designs using resistance or capacitance to slow circuit operation are unattractive from a fabrication or performance standpoint in modern CMOS. Triple Modular Redundancy (TMR) techniques, while well known, are costly in area and power. During the early 1990s, dual redundant techniques, which take advantage of the fact that Single Event Effects are transient, rather than permanent errors, were developed in several places. This RHBD design trend is not dependent on special process features. NASA-funded research at the University of New Mexico showed how insertion of delay elements might make these usable with single-string logic. We devised improved flip-flops that do not have the parasitic currents and indeterminate states of the University of New Mexico Whitaker cell. These are based on the Transition and Gate, also called a Guard Gate, on which Johnson Space Center has a patent. They can be used to construct dual redundant flip-flops such as the Dooley cell, or delay-based flop-flops that are more compact and able to accommodate preset or clear inputs, which the Whitaker cell is not.

## Guard Ring Effect on Set Pulse Width

A collaboration began in 2005 with researchers at Vanderbilt University who had done work on Guard Gates. One of the collaborators devised a technique for measuring the spectrum of Single Event Transient (SET) pulse widths very easily. All RHBD techniques depend, to some degree, on pulse widths, and the rate of change of pulse widths relative to technology process node became an area of much speculation. We published two papers last year showing the effect of completely enclosing cells with guard rings, as opposed to merely separating P and N regions with guard bands for latchup prevention (figure 1), and found that guard rings did reduce charge collection and pulse widths (figure 2).

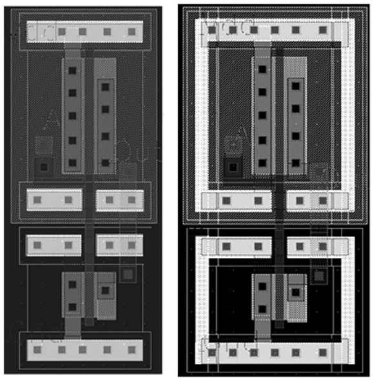

***Fig. 1.*** *Inverter layouts without and with guard bands.*

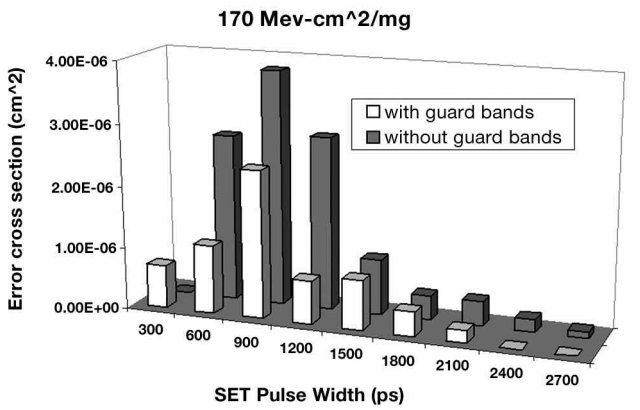


*Fig. 2. Error cross section as a function of pulse width for linear energy transfer (LET) of 170 MeV-cm²/mg. the use of an autonomous pulse-width measurement technique enabled such distributions to be obtained at all LETs.*

## Guard Drain Evaluation

The publication of the guard ring results prompted an evaluation using the SET measurement technique of the effectiveness of guard drains, a technique used in NASA ASICs but not formally evaluated and published (for example, see figure 3). These are expected to be even more effective than guard rings in actively suppressing charge collection. This work is ongoing, and will include development of revised ASIC standard cell libraries to include the Single Event Resistant Topology cell, a NASA-developed, conflict-free version of the Dooley cell.

## Digital Radio Applications

One of the candidate applications for this technology is digital radio. NASA desires that such applications be field reconfigurable, such as Software Defined Radio. One of the tools for doing this is large, SRAM-based FPGAs, about which we've already voiced concerns. There are two areas in which we seek innovative collaborators.

The first area is in applying RHBD techniques to the development of a reconfigurable device such as an FPGA, or perhaps of a more efficient architecture. The Department of Defense is working with Xilinx to develop an improved large-scale FPGA, but the upset rate will still be dozens per day or higher. Therefore, it will still require the TMR with scrubbing technique. This limits capacity too much to load modern applications into the device, and it greatly increases development costs.

The second area is in the development of computationally efficient modern radio protocols. Commercially available products may not be suitable for use in a limited-capacity, radiation-tolerant FPGA, or in a medium-scale ASIC. We have done work (not yet published) in developing Finite Impulse Response (FIR) filters using binary coefficients, which perform nearly as well as normal FIR filters, thus eliminating the need for large numbers of multipliers. This lends itself to incorporation into a very low power ASIC for use in portable battery-operated devices.

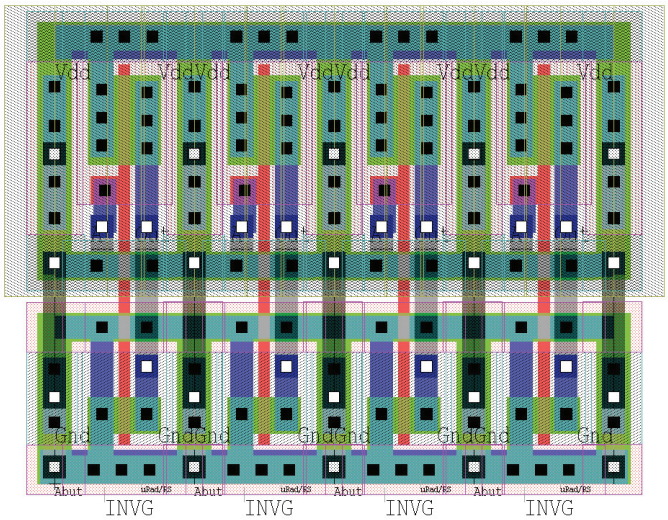


*Fig. 3. A group of four inverters illustrates vertical separation by guard drains.*